Abstract

A gold code generator is described comprising two pairs of linear feedback shift registers, the seed values for the second pair of linear feedback shift registers are different from the seed values for the first pair of linear feedback shift registers. The second seed values are calculated from the first seed values. The use of this second pair of linear feedback shift registers prevents the need to use a wide span of taps to the linear feedback shift register to produce output bits. By using two pairs of linear feedback shift registers, a parallel output implementation can be produced in which multiple output bits are produced in a single clock cycle.